



ALPHA & OMEGA
SEMICONDUCTOR

AON7200

30V N-Channel MOSFET

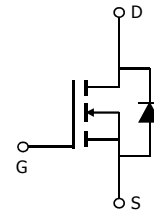
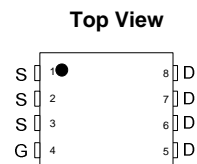
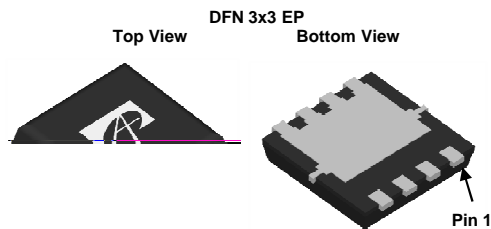
General Description

The AON7200 uses trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Conduction and switching losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and C_{rss} .

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 8m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 11m Ω

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.85	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	146			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		6.7 9.2	8 11	mΩ
		V _{GS} =4.5V, I _D =15A		9	11	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		60		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	870	1090	1300	pF
C _{oss}	Output Capacitance		340	490	640	pF
C _{rss}	Reverse Transfer Capacitance		22	38	53	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.4	0.9	1.4	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A	12	16	20	nC
Q _{g(4.5V)}	Total Gate Charge		5	7	9	nC
Q _{gs}	Gate Source Charge		2	2.5	3	nC
Q _{gd}	Gate Drain Charge		1.5	2.5	3.5	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			2		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	10	13	16	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	20	25	30	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

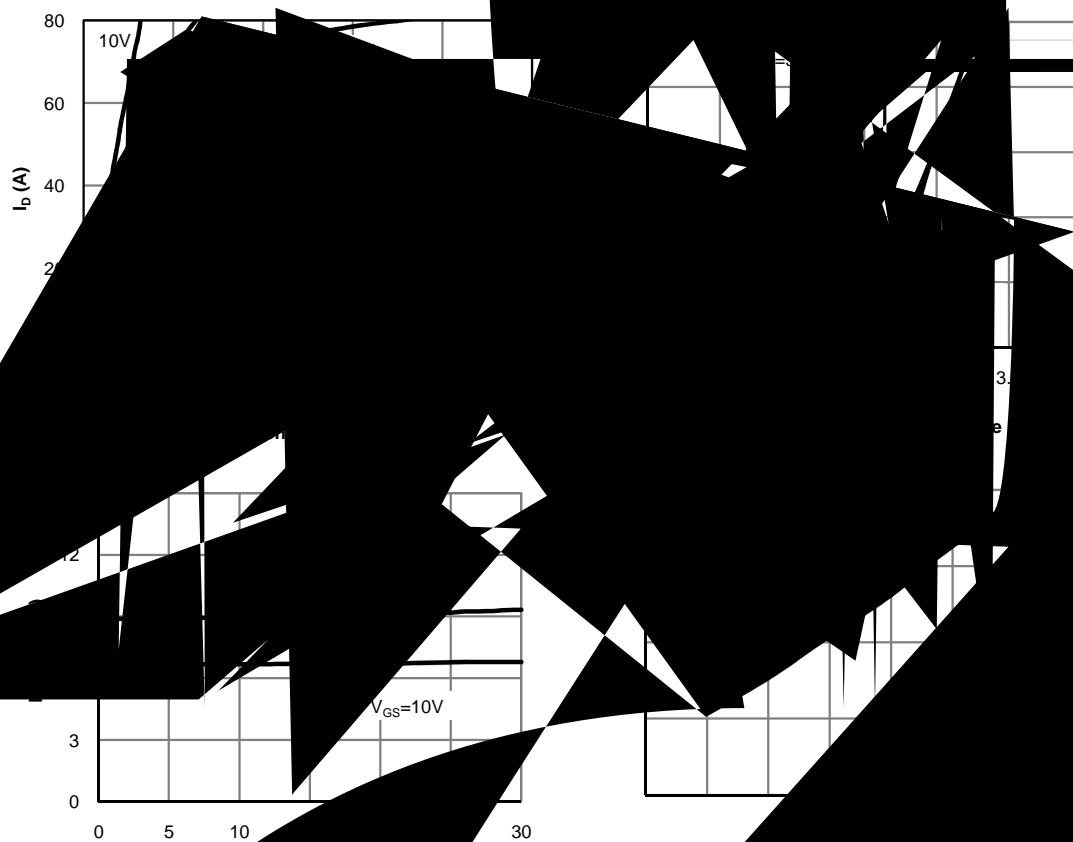


Figure 3: On-Resistance vs. Drain Current and Gate Voltage



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

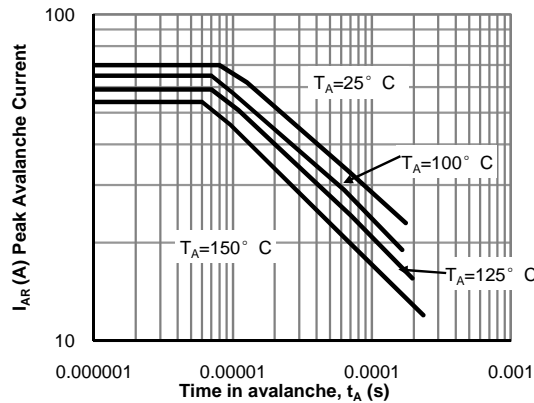


Figure 12: Single Pulse Avalanche capability (Note C)

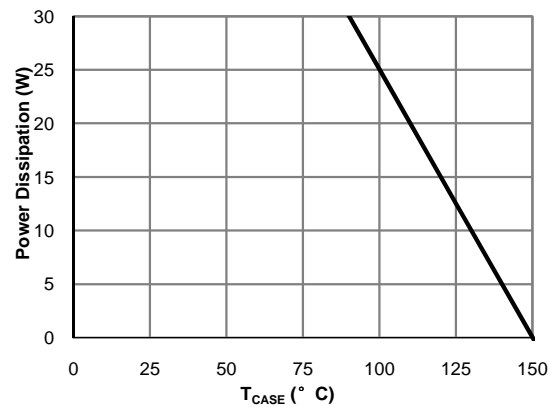


Figure 13: Power De-rating (Note F)

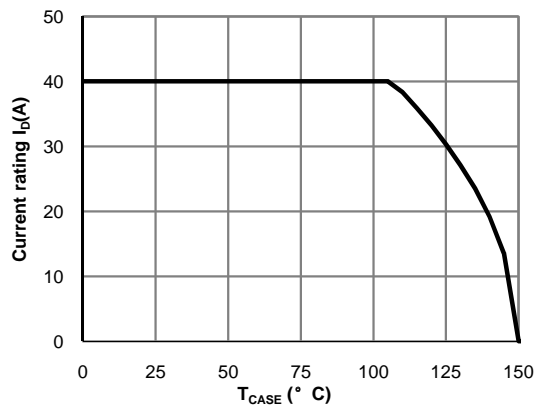


Figure 14: Current De-rating (Note F)

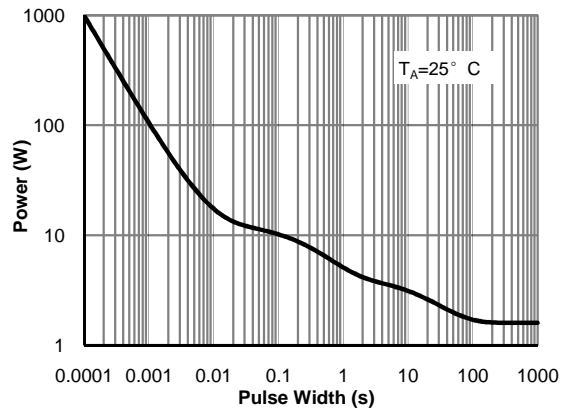


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

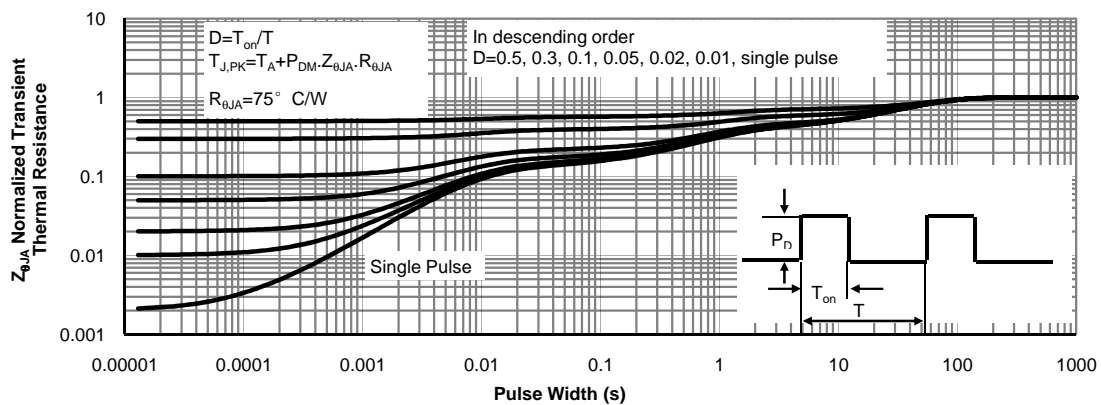
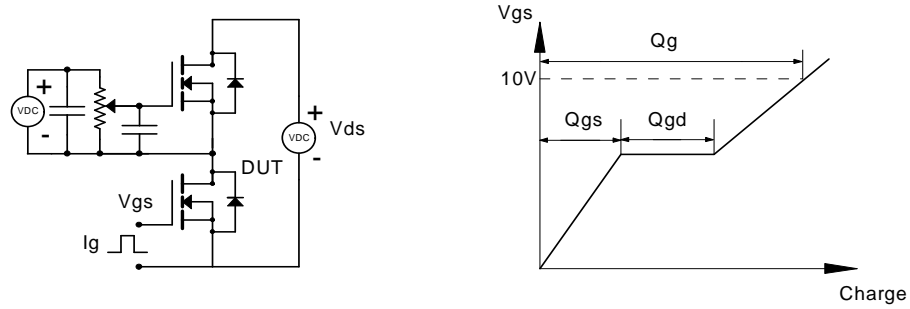


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

